

# ADHA: Automatic Data layout framework for Heterogeneous Architectures

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## ABSTRACT

Data layouts play a crucial role in determining the performance of a given application running on a given architecture. Existing parallel programming frameworks for both multicore and heterogeneous systems leave the onus of selecting a data layout to the programmer. Therefore, shifting the burden of data layout selection to optimizing compilers can greatly enhance programmer productivity and application performance. In this work, we introduce ADHA: a two-level hierarchical formulation of the data layout problem for modern heterogeneous architectures. We have created a reference implementation of ADHA in the Heterogeneous Habanero-C (H2C) parallel programming system. ADHA shows significant performance benefits of up to  $6.92\times$  compared to manually specified layouts for two benchmark programs running on a CPU+GPU heterogeneous platform.

## Categories and Subject Descriptors

D.3.4 [Software]: PROGRAMMING LANGUAGES—*Processors, Compilers*

## Keywords

Compilers, Data Layout, Heterogeneous Architectures

## 1. INTRODUCTION

In recent years, the end of Dennard scaling has brought about significant changes in the fundamental processor design. We are now entering an era of heterogeneous and specialized processors, and this trend is expected to continue in the future. One dominant heterogeneous architecture found in many systems today is a CPU+GPU system. The processor architecture, the memory hierarchy and cache structures are significantly different on the CPU and GPU sides. With such diverse characteristics, it not only hard to program these systems in a portable manner, but also quite challenging to optimize them.

One major factor which impacts performance is the data layout [4, 5]. The choice of a good data layout depends on

several factors including target machine parallelism, memory hierarchy, data access patterns, and input size. An application program with multiple data-parallel kernels can map each kernel onto any of the heterogeneous processors. It is hard for the programmer to determine if a single layout is best for all the kernels or if a better choice is to select different data layouts for different kernels with data remapping operations performed in between kernels. Also, the programmer has to manually re-write the code for each data layout combination even to just evaluate the best data layout. The number of combinations increase exponentially with the number of kernels and the number of fields accessed by each kernel increase.

To overcome this limitation, we design ADHA: a two-level compiler based automatic data layout framework and a reference implementation of the same in the Heterogeneous Habanero-C [2] (H2C) programming system. The lower level formulation deals with the data layout problem for a parallel code region, and provides a greedy algorithm that uses an *affinity graph* to obtain approximate solutions. The higher level formulation targets data layouts for the entire program, for which we provide a graph-based shortest path algorithm that uses the data layouts for the code regions computed in the lower level. In this work, we consider only *AoS (Array of structure)* and *SoA (Structure of Array)* layouts.

## 2. OVERALL FRAMEWORK

We denote a data/task-parallel operation that is executed either on the CPU or on the GPU as a **section**. A H2C program may consist of several *forasync* parallel loop constructs, each of which constitutes a **section** of its own.

Our automatic data layout framework, ADHA, consists of two steps. The first step consists of a greedy strategy with the goal of determining the "optimal data-layout of a section" or simply **ODS**. The key idea is to construct an affinity graph for a H2C program where the "nodes" of the affinity graph represent the fields (and arrays) being accessed in the section and the "edges" represent the affinity between two fields. The affinity weight of an edge is computed based on the number of common occurrences between the two nodes involving the edge. Once the affinity graph is constructed, we employ a greedy clustering algorithm to cluster the fields. The cluster size is determined based on the underlying architecture (e.g., cache size and memory hierarchy). The result of the clustering algorithm is used to combine the fields in structures.

The next step involves finding the best data-layout for the entire H2C program (denoted as "program data-layout")

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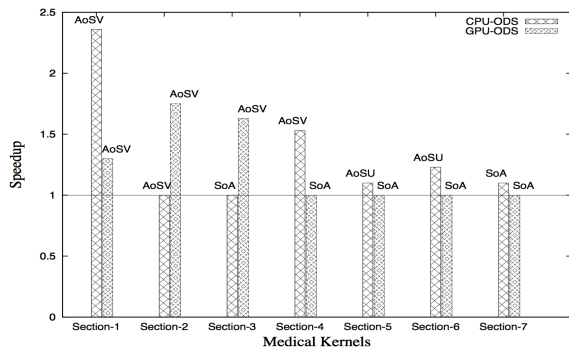


Figure 1: Speedup of the Medical sections

or simply PDL) from the computed best data layouts for each section. First, we construct a control flow graph for each section (denoted as SCFG). We then construct a rooted directed acyclic graph with the first section as the root. Each pair of sections either share two edges, namely the combine edge and the remap edge, or none. The edge weight of the combine edge represents the loss in performance due to combining the two sections involving the edge and assigning an intermediate data layout. The data layout of the combined sections is obtained running the ODS pass on the merged section.

The remap edge weight is the cost of remapping from the parent section to the child section, which is computed based on the number of common fields in the two sections. We then employ the shortest path algorithm to determine the best data layout for the entire program. For the PDL pass, we provide a tuning profile of the execution times of both the CPU and GPU (since we do not perform the mapping automatically). The output of the PDL pass gives us the best data layout along with the mapping to the CPU or the GPU.

Our implementation of ADHA automatically compiles forasync loops down to OpenCL with the corresponding data layout output by the ODS + PDL pass. ADHA can be employed to efficiently run a H2C program on modern CPU+GPU platforms that support OpenCL.

### 3. EXPERIMENTAL EVALUATION

We evaluated our implementation of ADHA with two benchmarks arising from different domains as summarized in Table 1. #S denotes the number of sections and #F denotes the number of fields in the entire program. Medical is from the CDSC benchmark suite [1] and K-Means is from the Rodinia suite [3].

Description	#S	#F	Input
Medical Image Registration	7	6	256×256×256
K-Means Clustering Algorithm	2	32	8388608

Table 1: Benchmarks Description

The experiments were conducted on a Intel-X5660 CPU with 6 cores running at 2.8GHz and a NVIDIA Tesla-M2050 GPU with 8 SMs running at 575 MHz. We use gcc version 4.4.6 with O2 optimization level. For each of the benchmarks, we executed the OpenCL code with the original data layout and with the automatically generated layout from ADHA on both the CPU and GPU.

Medical image registration consists of 7 sections. Sections(1-3) have heavy control flow and do not vectorize while sections(4-7) are vectorizable. Table 2 shows the fields accessed by all

the sections and the different data layouts generated by the ODS pass for each of the sections. For instance, AoSU lays out fields  $V1, V2, V3, S, T$  and  $interpT$  as individual arrays using SoA layout and interleaves the fields  $U1, U2, U3$  using an AoS layout. Figure 1 shows the speedup from the data

Data Layout	Description
SoA	$V1, V2, V3, U1, U2, U3, S, T, interpT$
AoSU	$V1, V2, V3, \{U1, U2, U3\}, S, T, interpT$
AoSV	$\{V1, V2, V3\}, U1, U2, U3, S, T, interpT$

Table 2: Medical Imaging ODS Data Layouts

layout generated by the ODS pass compared to the original SoA layout by executing the seven sections on CPU and GPU. ODS pass performs better for most of the sections on the CPU. On the GPU, the SoA layout performs the best for sections-(4-7) due to memory coalescing. The GPU benefits from cache locality for sections-(1-3).

Platform	Layout Description	Speedup
CPU-ODS	32 Fields belong to SoA	5.5
GPU-ODS	4 AoS of size 8 each	1

Table 3: KMeans Section-1 ODS and Speedup

The benchmark *K-Means* consists of two sections: the first section is a data parallel loop while the second section performs reduction on all the features. The second section is executed sequentially in the original implementation, owing to the difficulty of implementing reduction over varying number of variables using OpenCL. The original data layout for both these sections is SoA. The first section CPU-ODS is an AoS layout and the GPU-ODS is SoA layout and are shown along with their speedups in Table 3. The AoS layout which is the output from the ODS pass for the second section improves its performance by a factor of  $8\times$ . This is because the second section suffers a lot of cache misses due to the SoA layout.

Table 4 provides the speedup obtained by the overall data-layout from the PDL pass. As stated before, the PDL pass gives the mapping onto CPU or GPU along with the data-layout. For the Medical benchmark, sections-(1-3) are mapped onto the CPU with AOSV layout and then a remap operation is performed to SOA layout with sections-(4-7) mapped to the GPU. *K-Means* sections-(1-2) are both mapped onto the CPU with a combined AoS layout.

Benchmark	section Mapping SCFG	Speedup
Medical	CPU-ODS(1-3) remap GPU-ODS(4-7)	1.34
K-Means	CPU-ODS combine CPU-ODS	6.92

Table 4: PDL Speedup for Medical and K-Means

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